

Fig.1

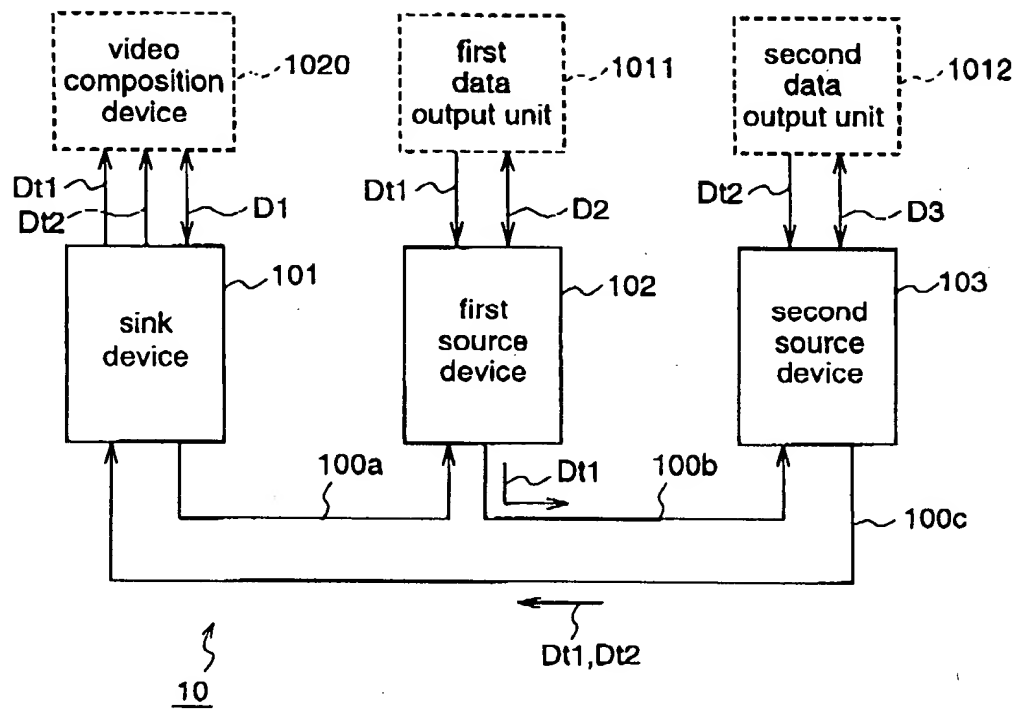


Fig.2 (a)

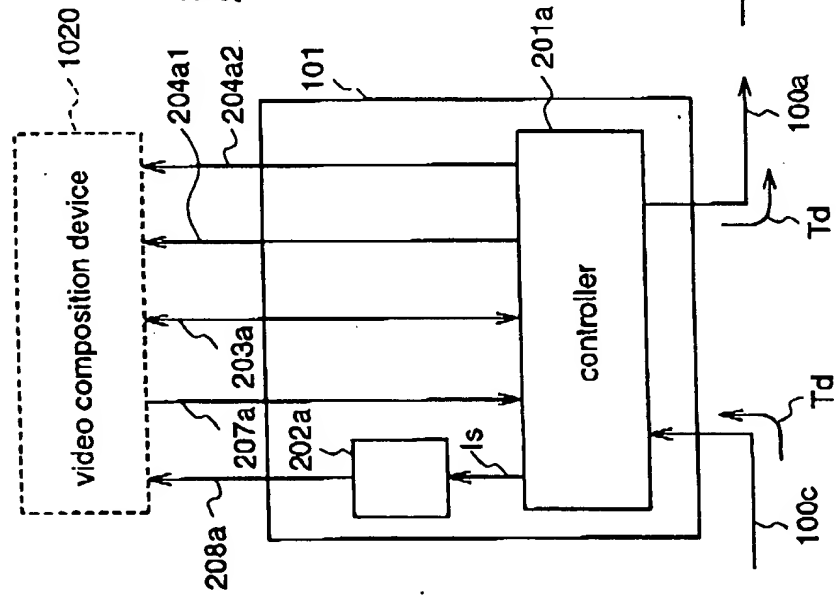


Fig.2 (b)

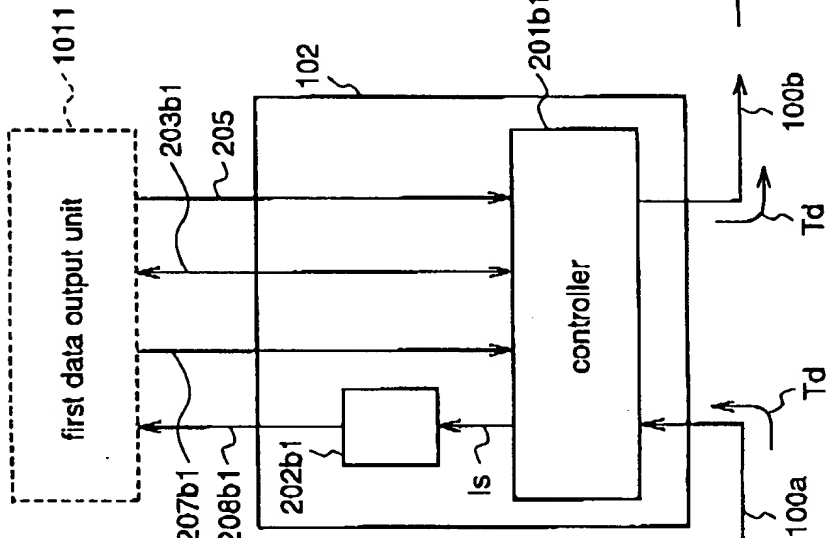


Fig.2 (c)

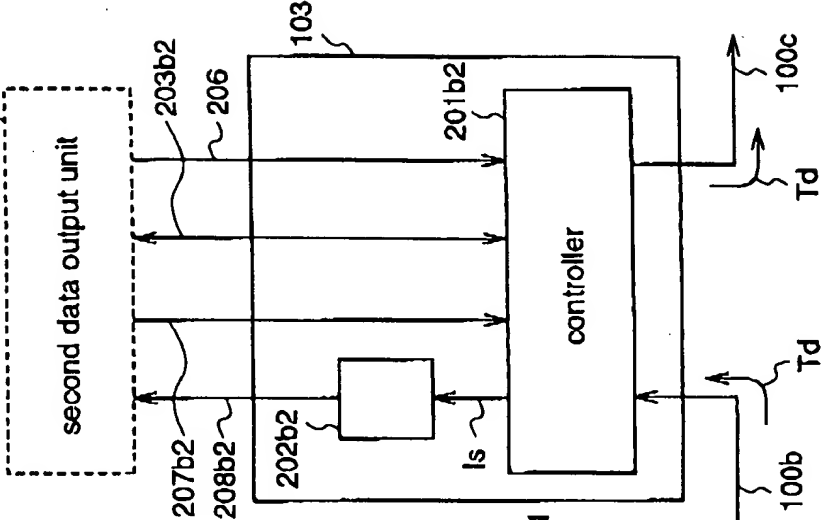


Fig.3

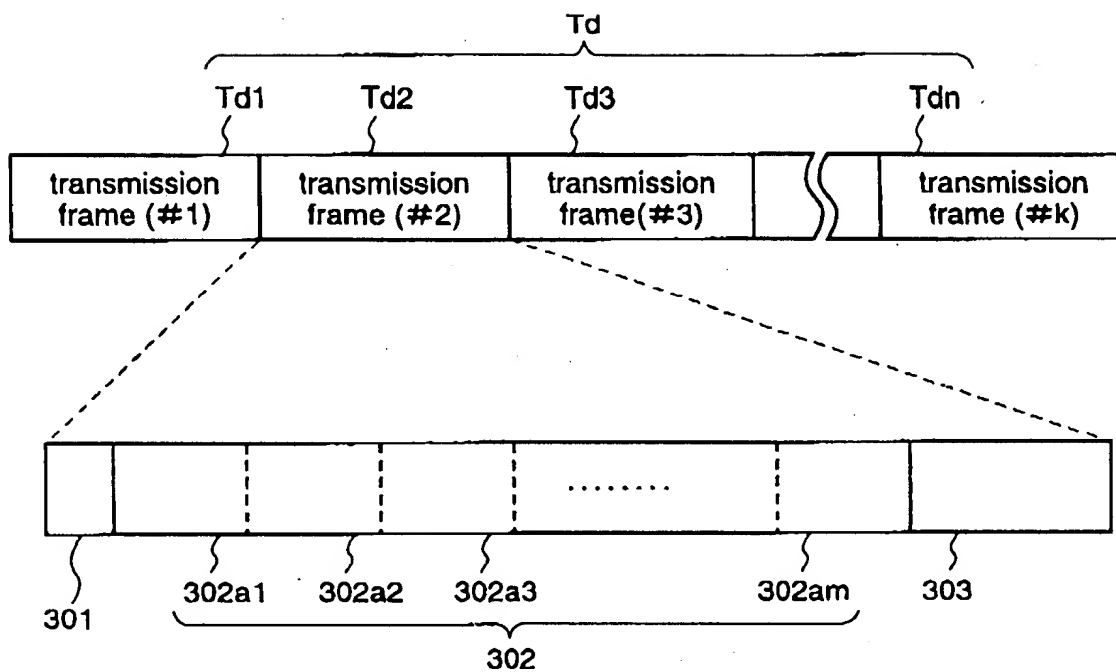


Fig.4 (a)

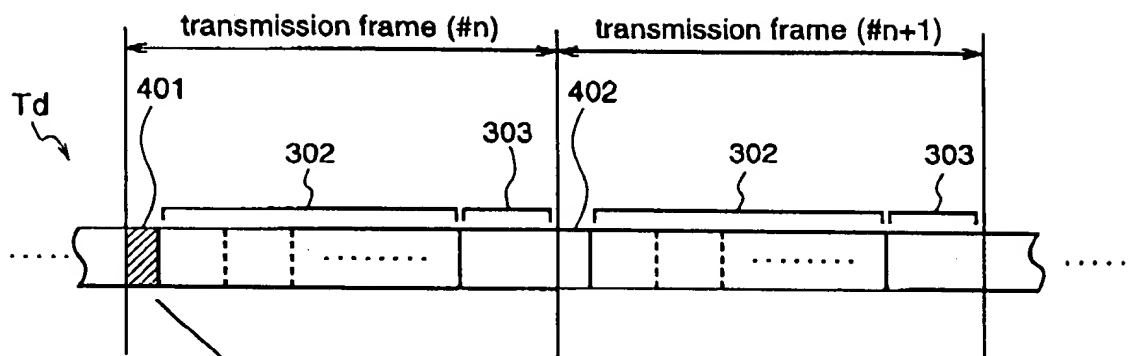
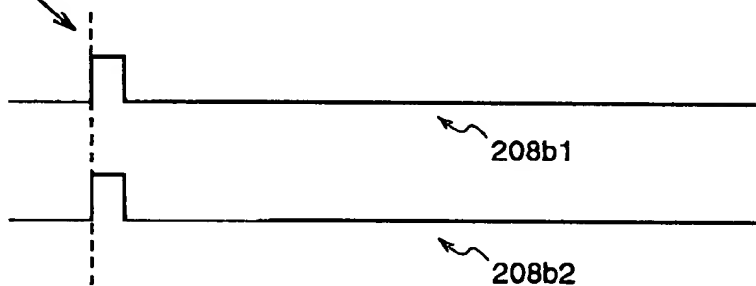


Fig.4 (b)

Fig.4 (c)



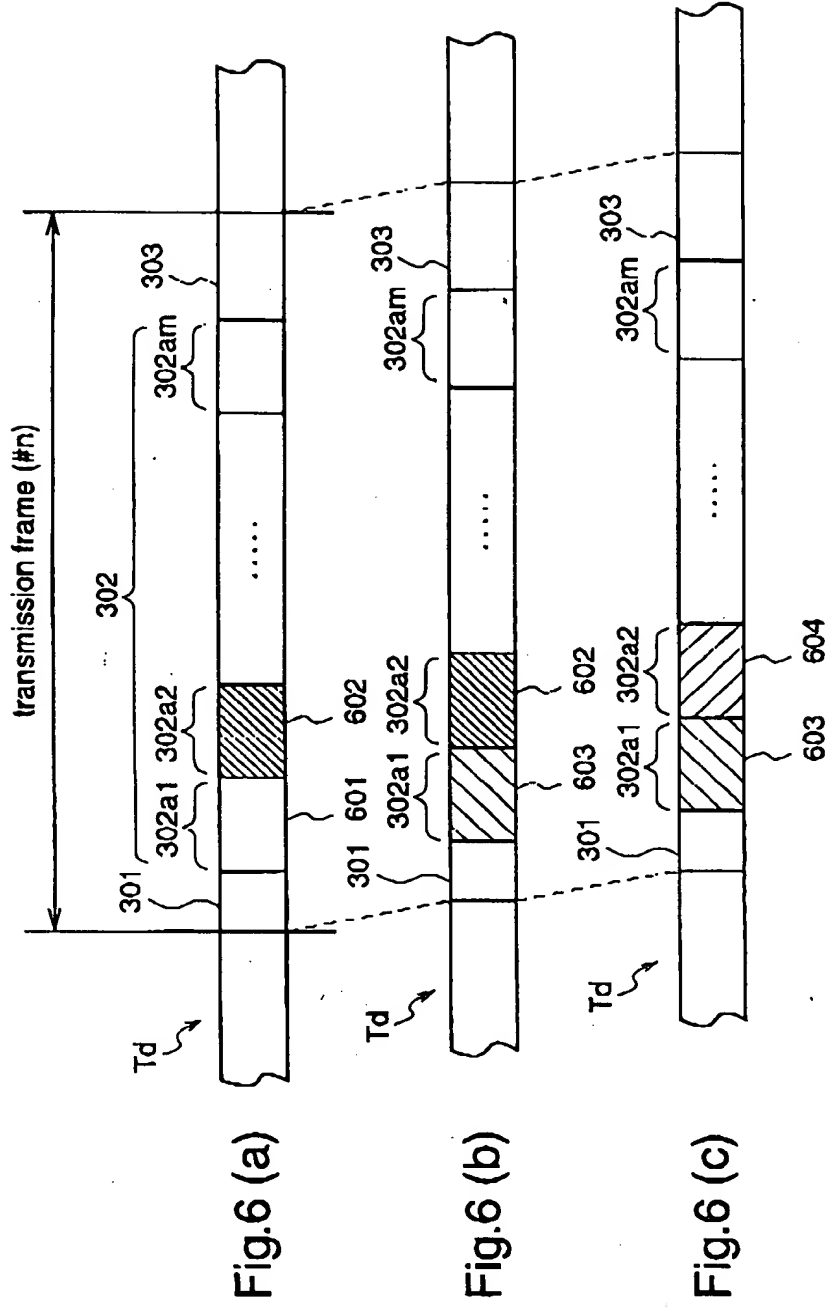


Fig.7

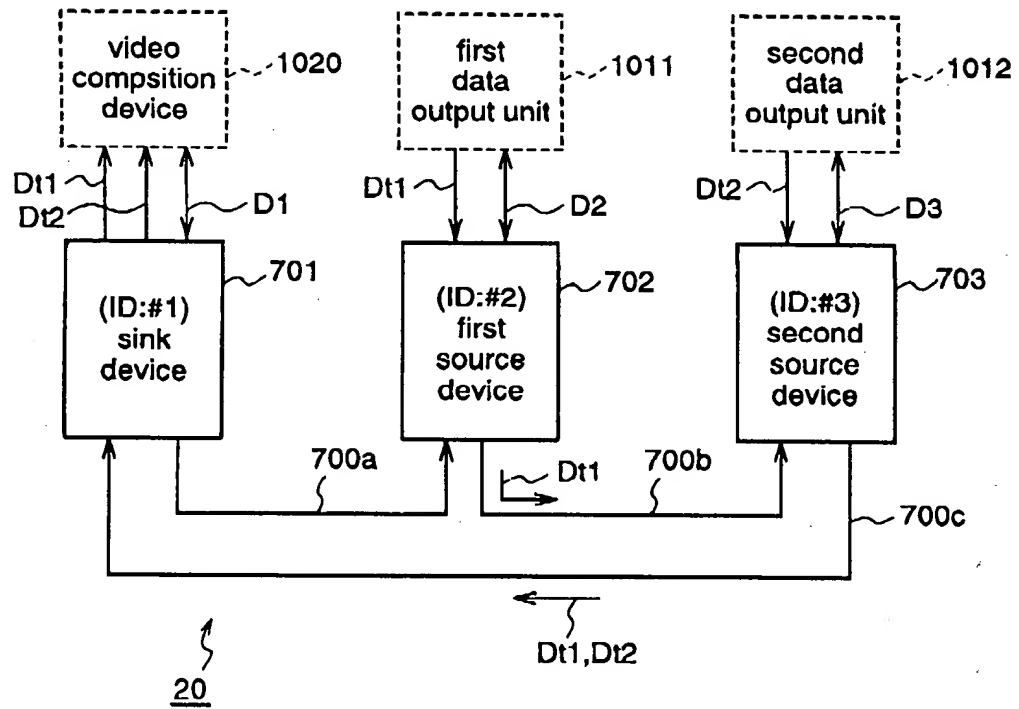


Fig. 8 (a)

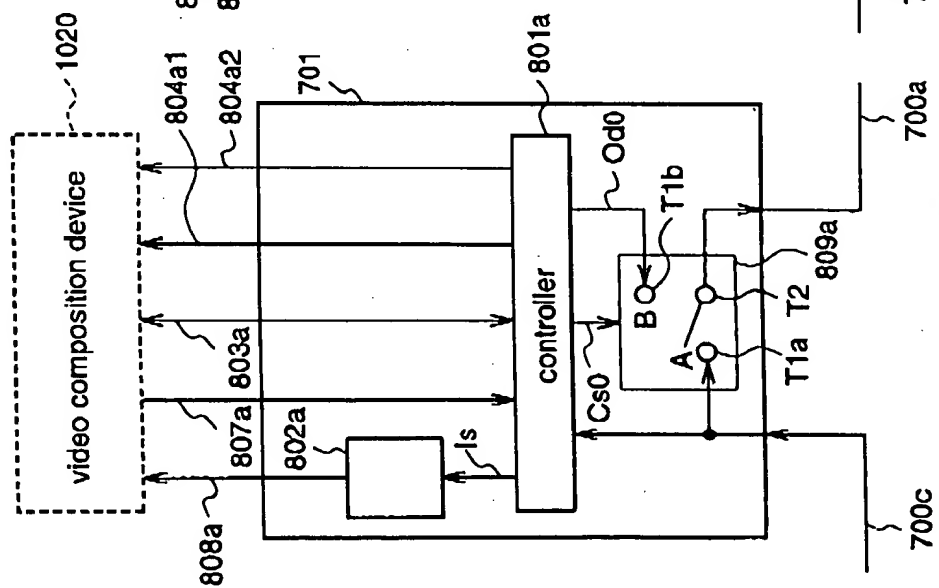


Fig. 8 (b)

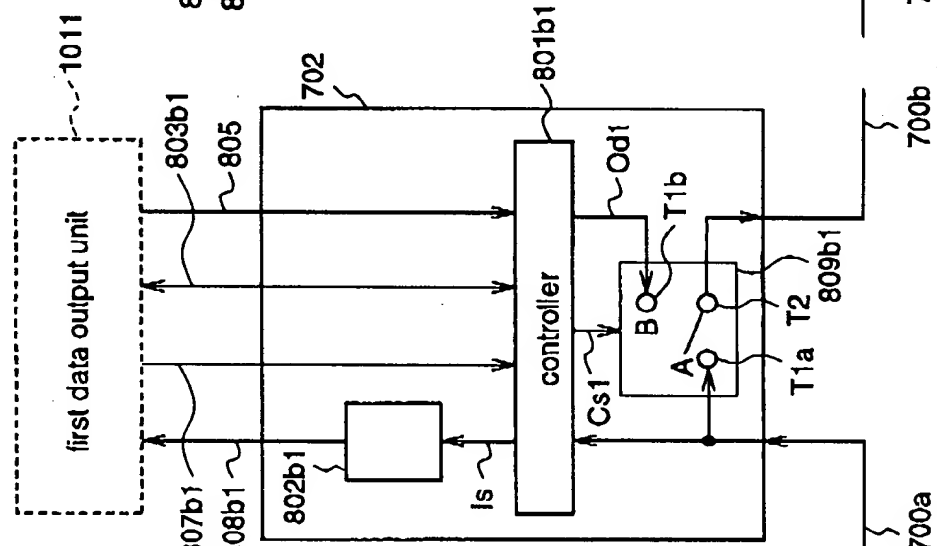


Fig. 8 (c)

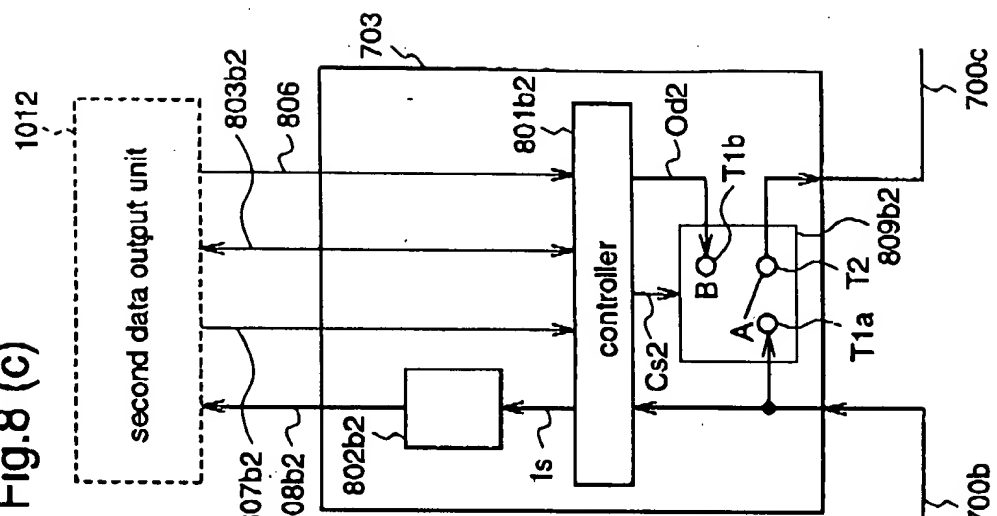


Fig.9

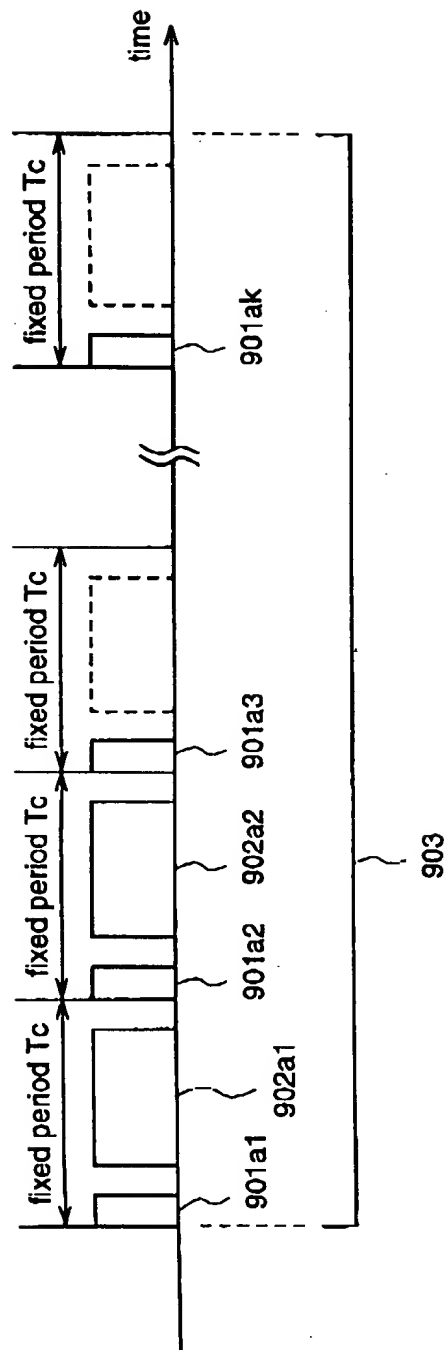


Fig.10 (a)

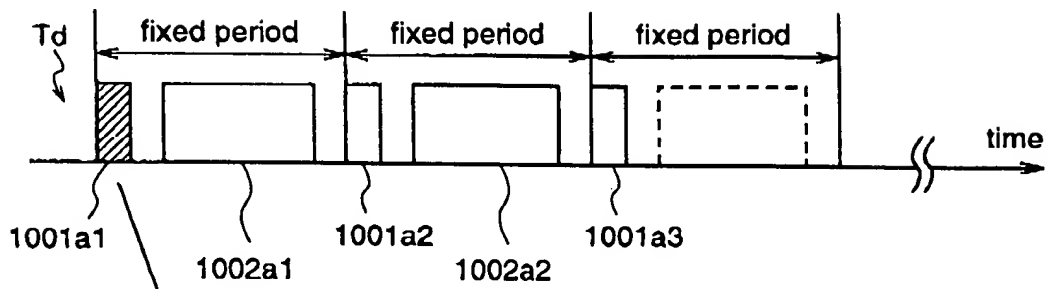
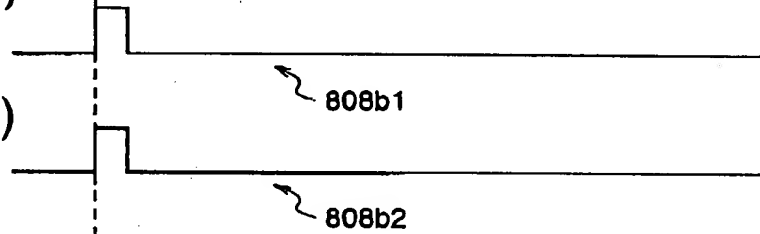


Fig.10 (b)

Fig.10 (c)



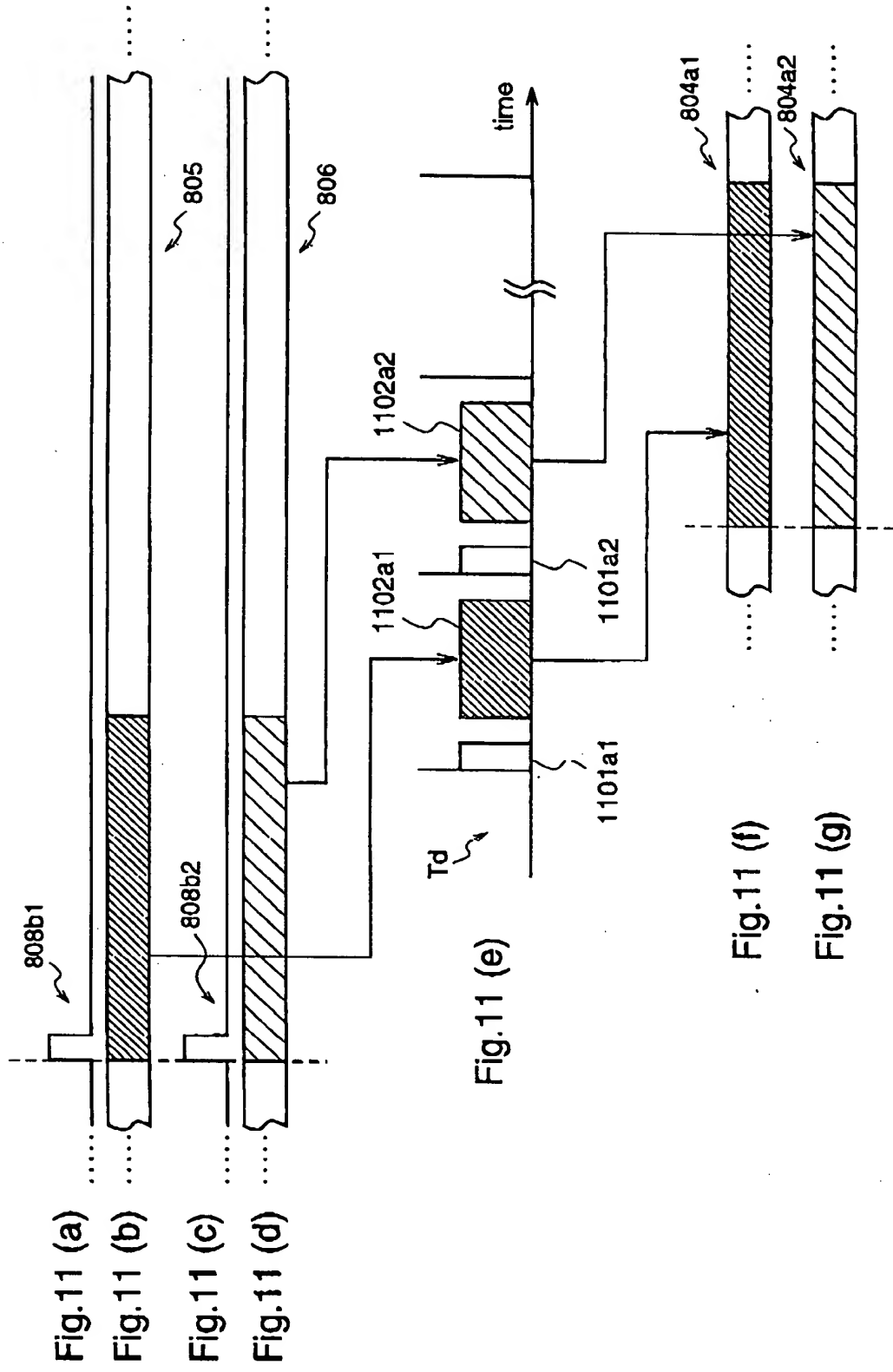


Fig.12

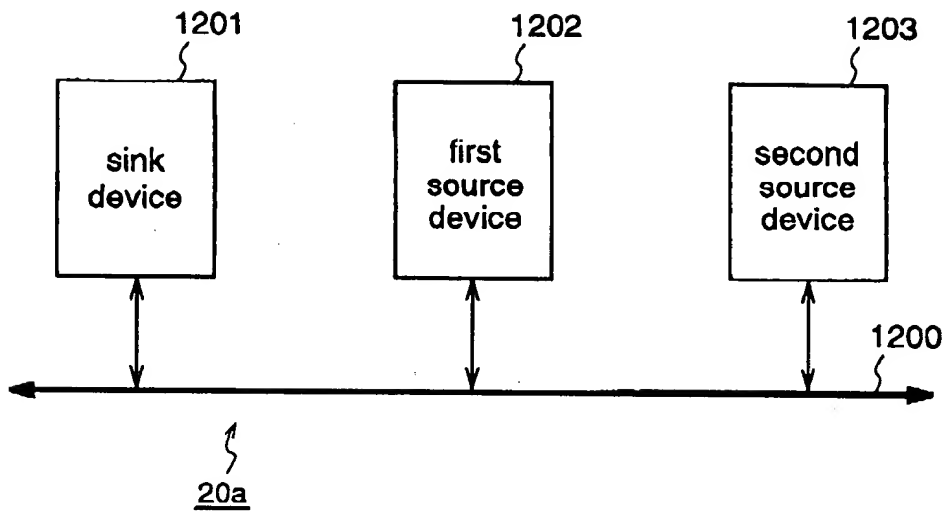


Fig.13

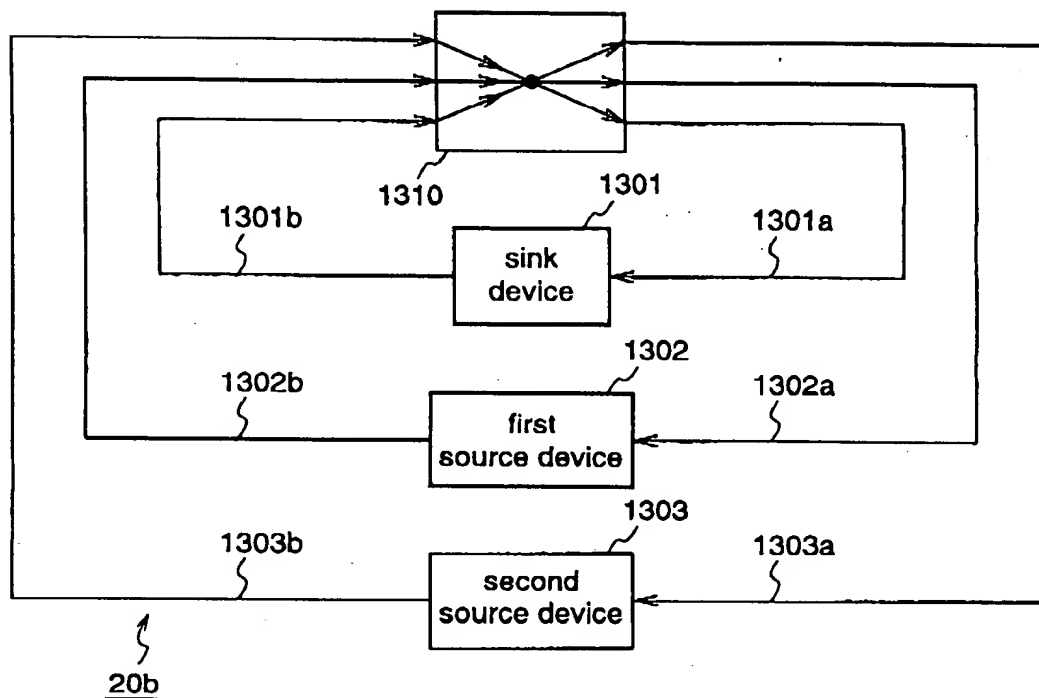


Fig.14

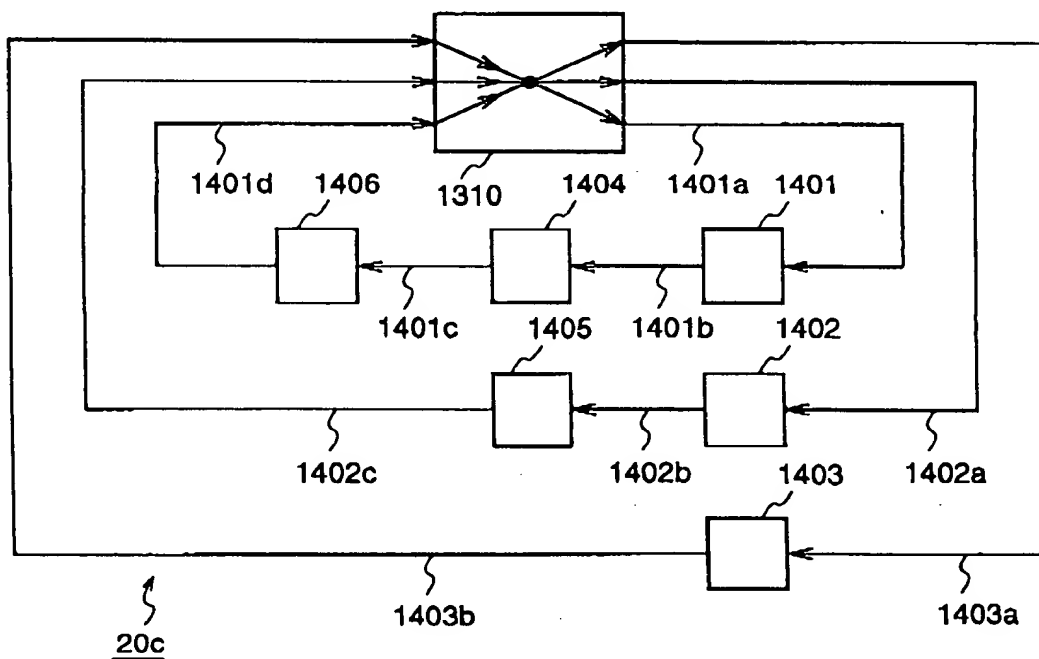


Fig.15

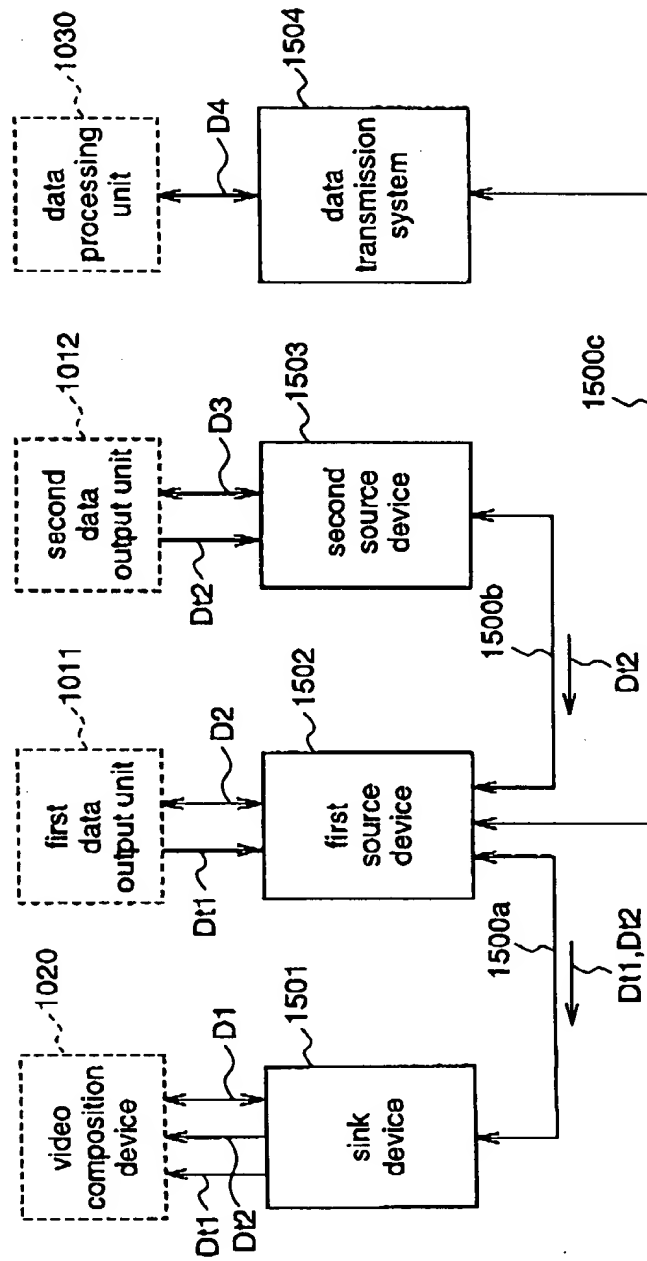


Fig.16 (a)

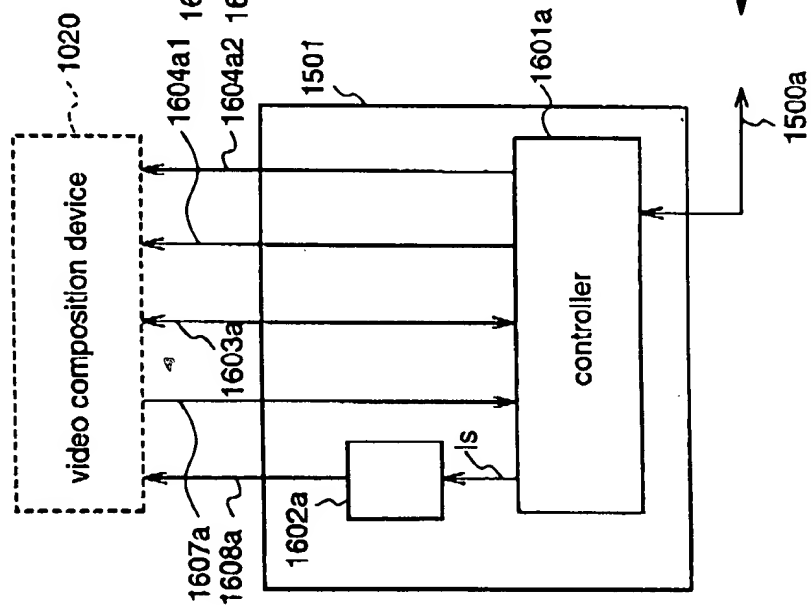


Fig.16 (b)

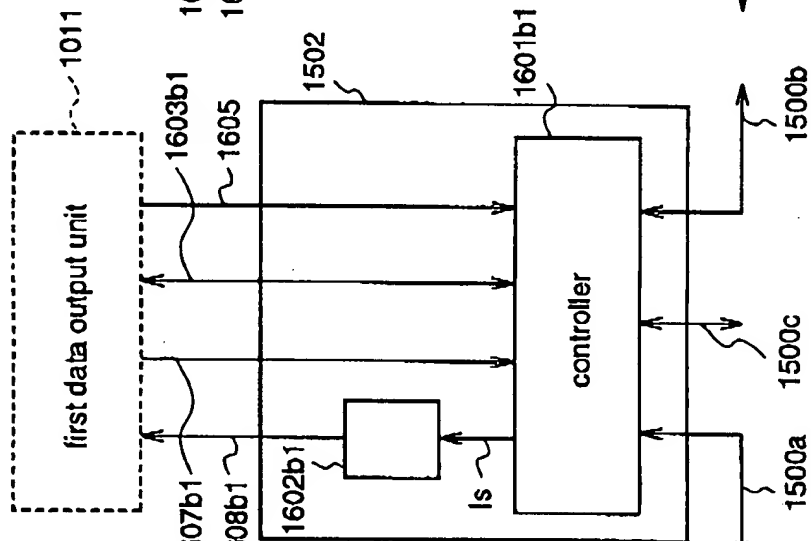


Fig.16 (c)

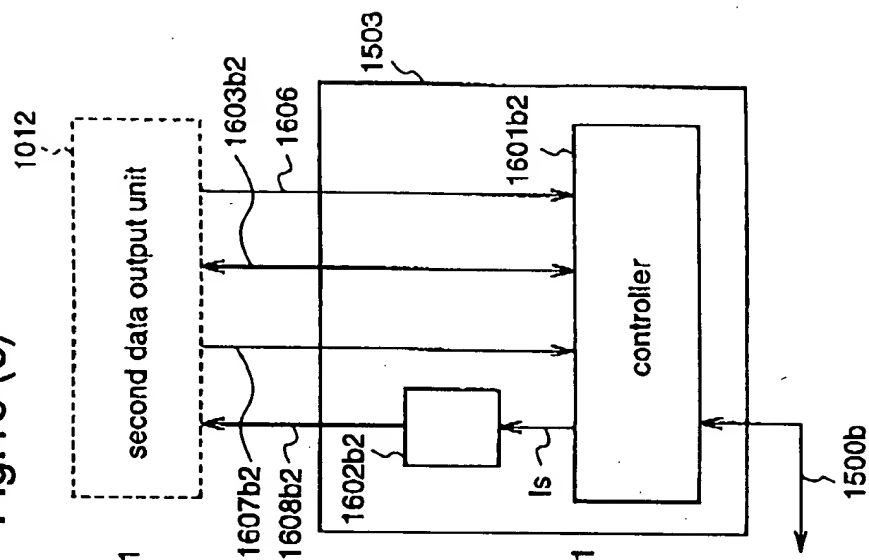
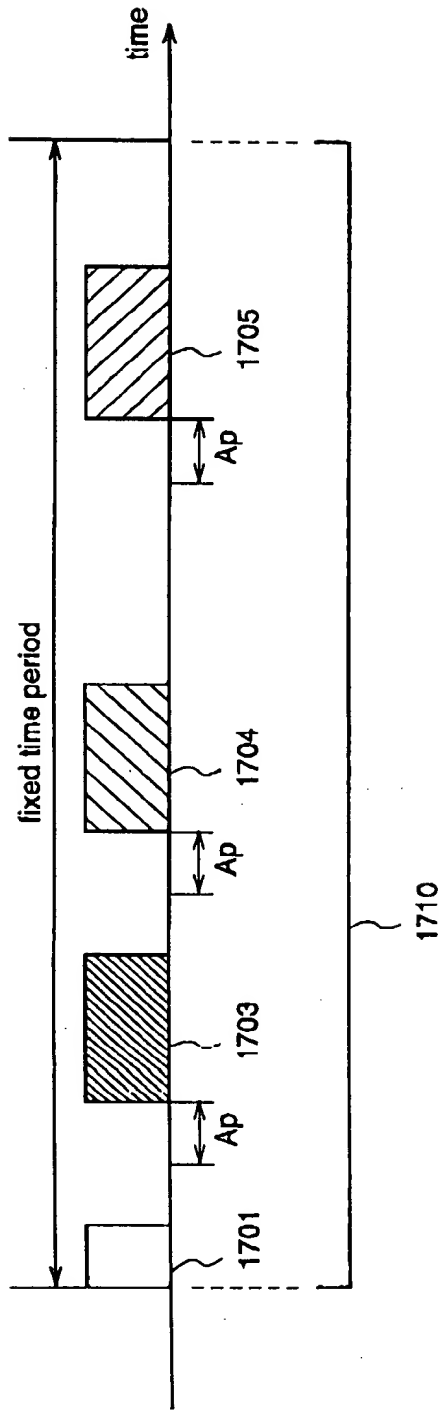
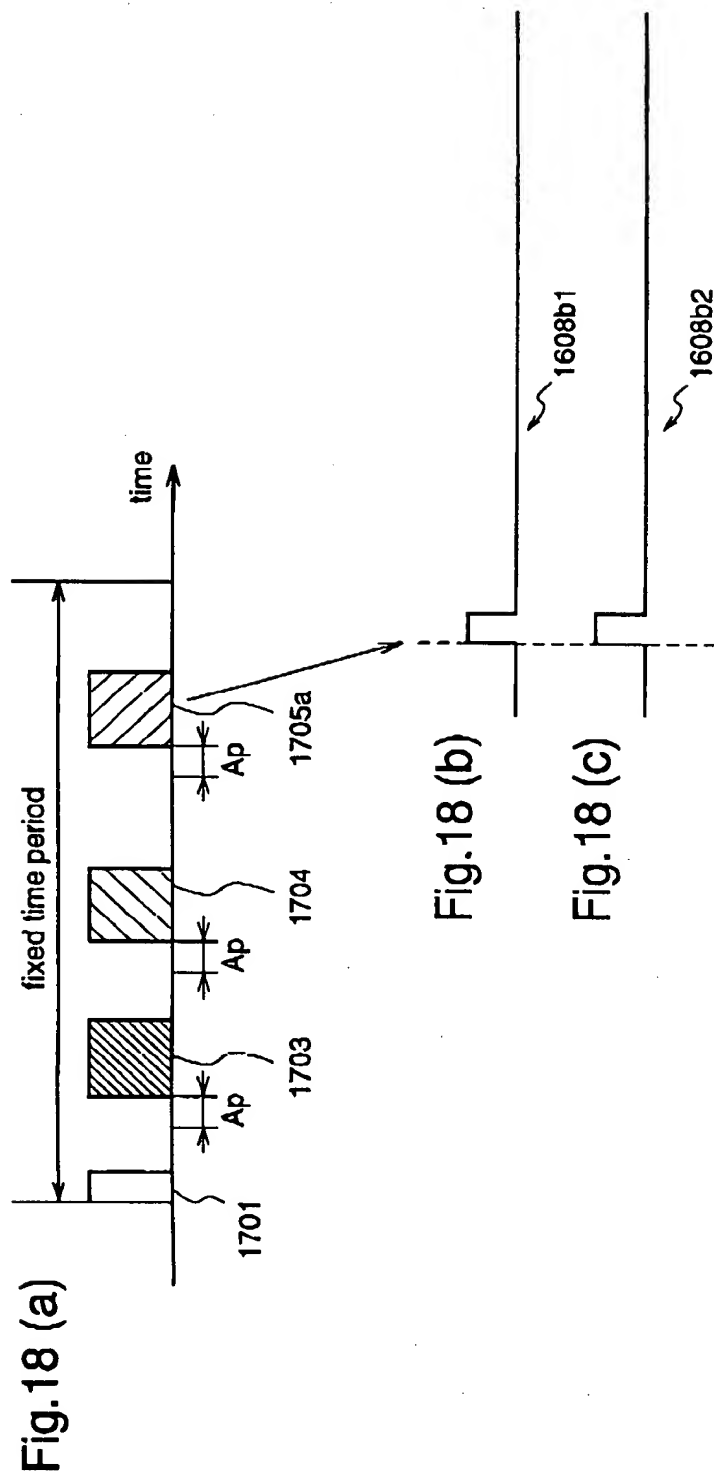


Fig.17





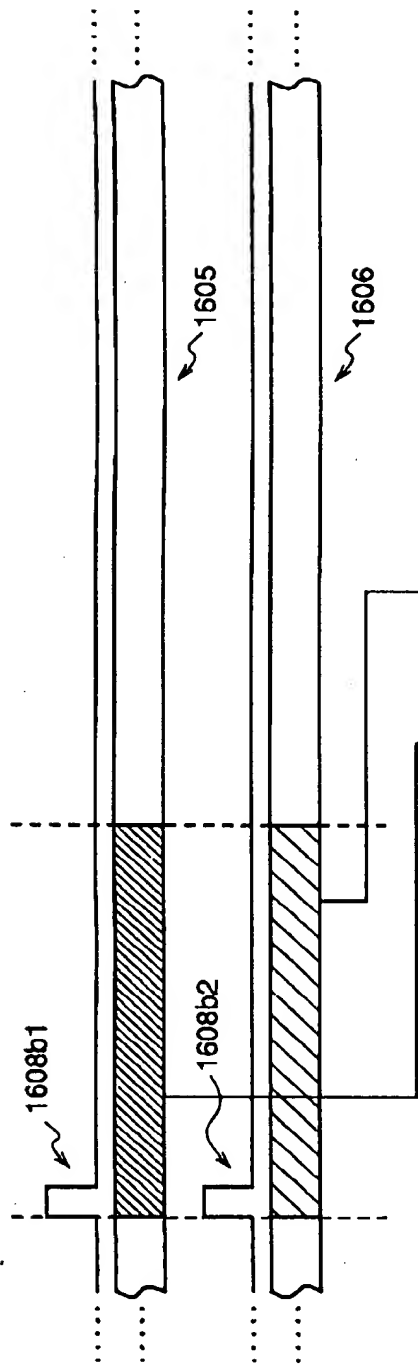


Fig. 19 (a)

Fig. 19 (b)

Fig. 19 (c)

Fig. 19 (d)

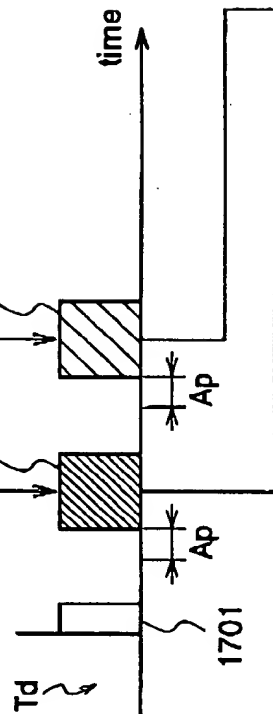


Fig. 19 (e)

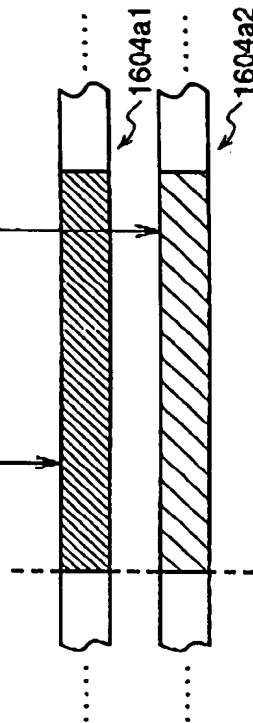


Fig. 19 (f)

Fig. 19 (g)

Fig.20

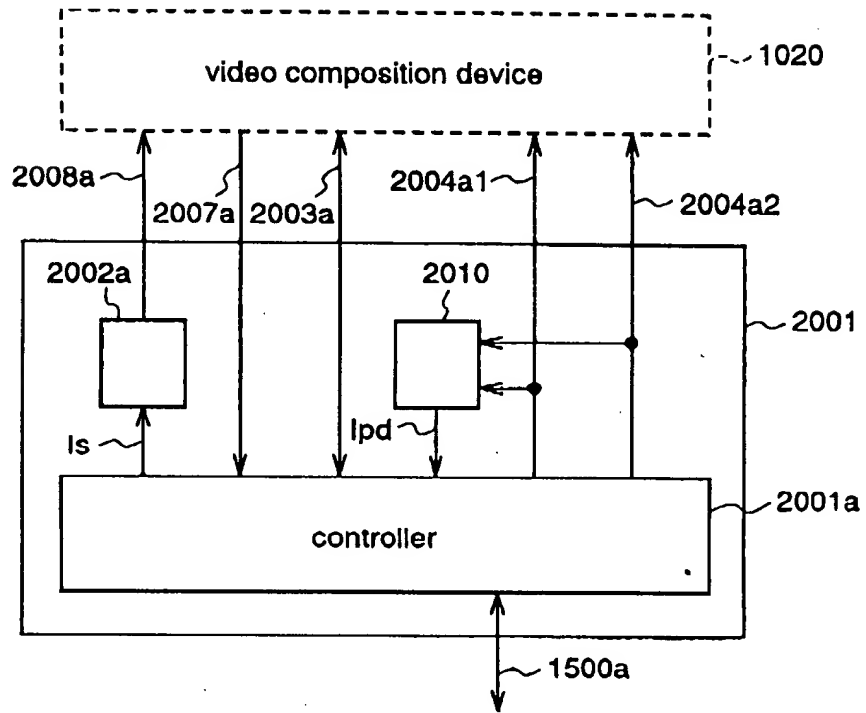


Fig.21 (a)



Fig.21 (b)

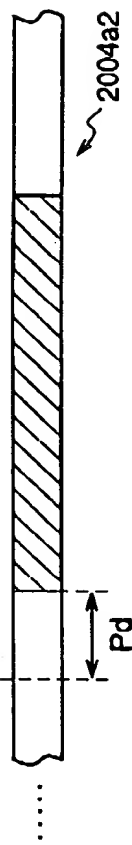


Fig.21 (c)



Fig.21 (d)

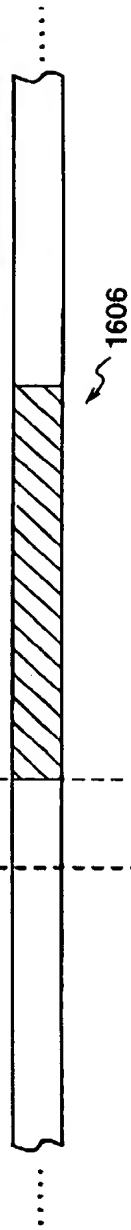


Fig.21 (e)

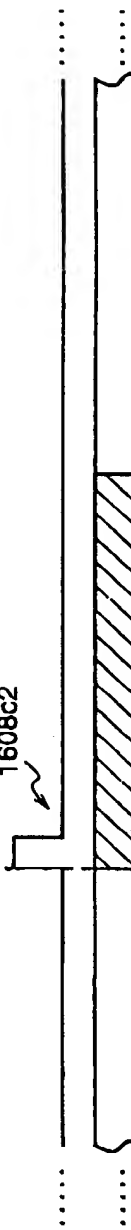


Fig.21 (f)

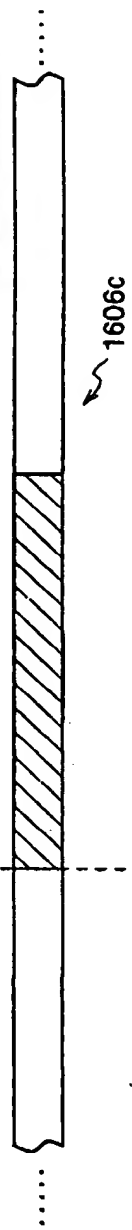


Fig.22

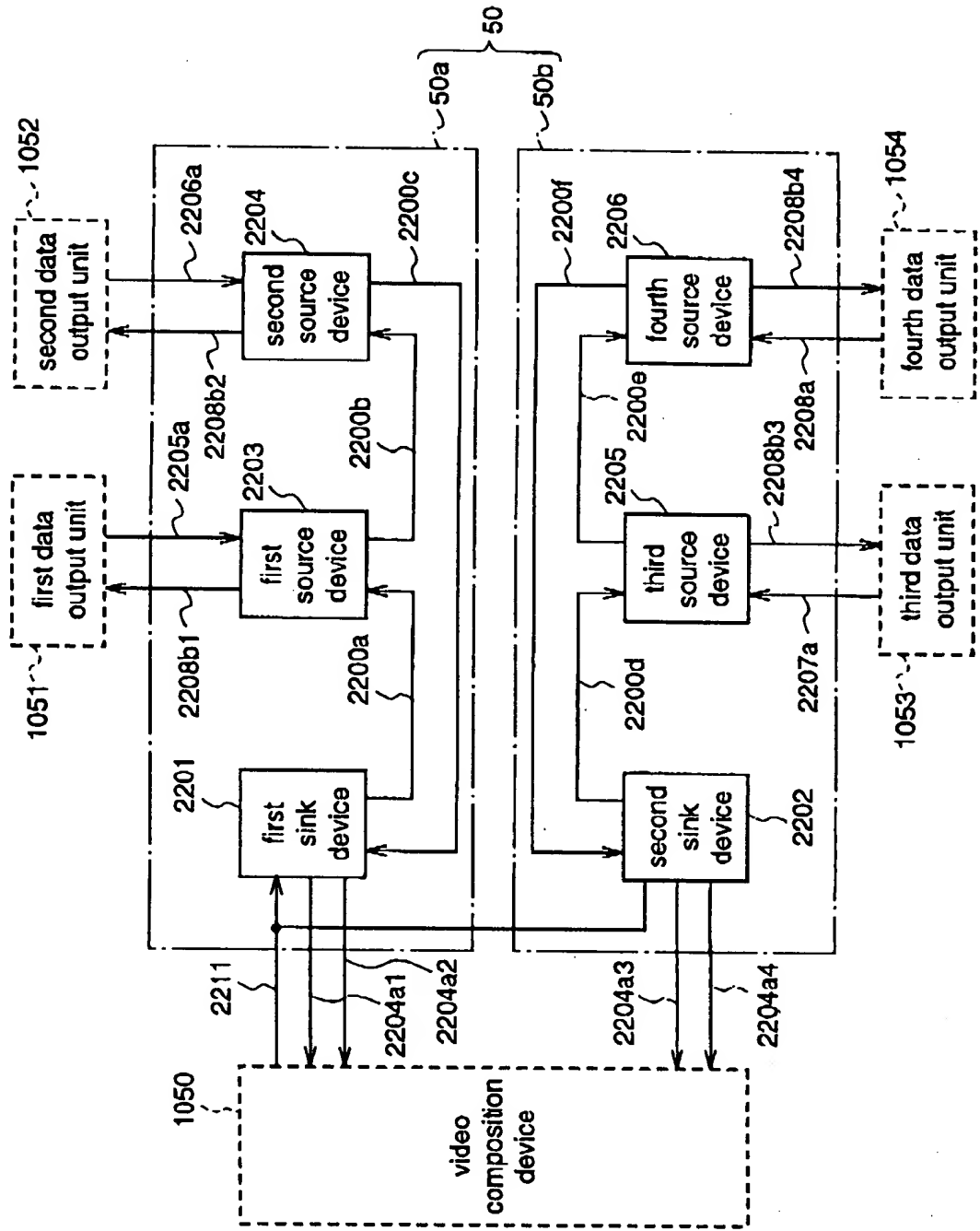


Fig. 23

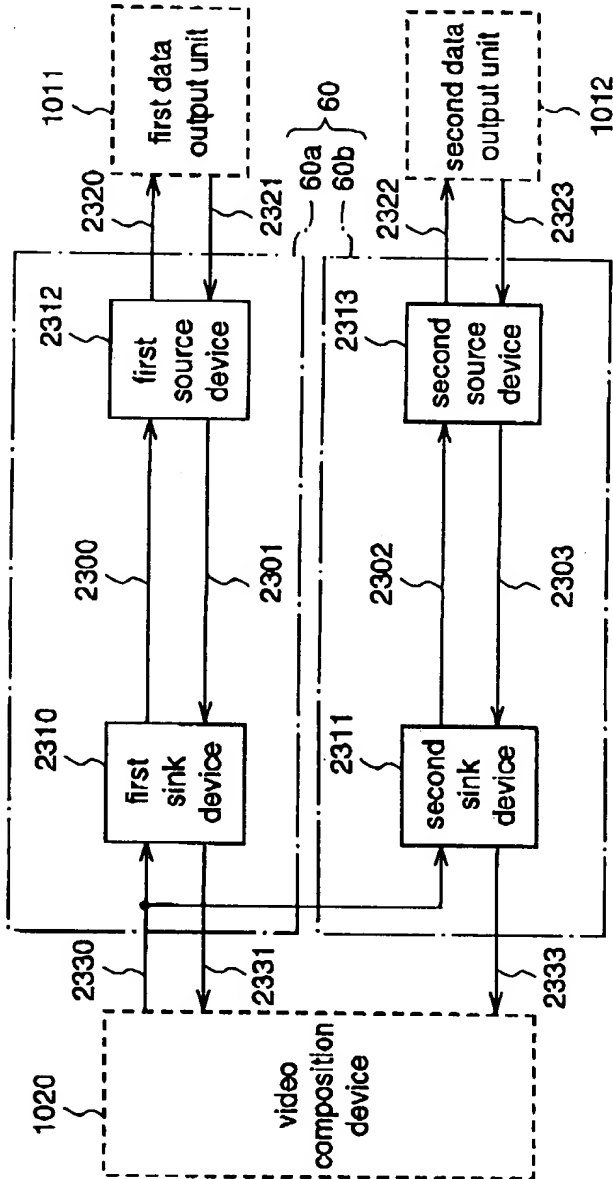


Fig.24 (a)

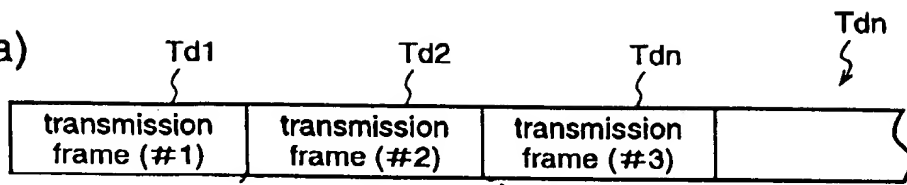


Fig.24 (b)

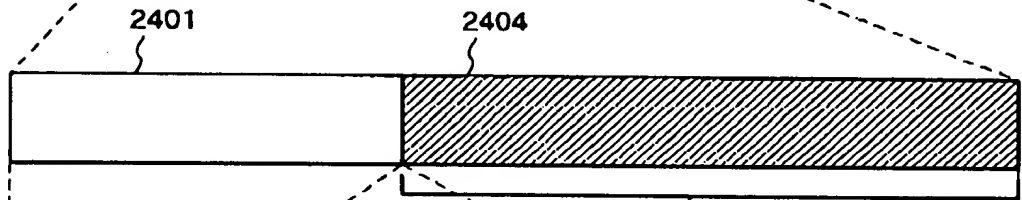


Fig.24 (c)

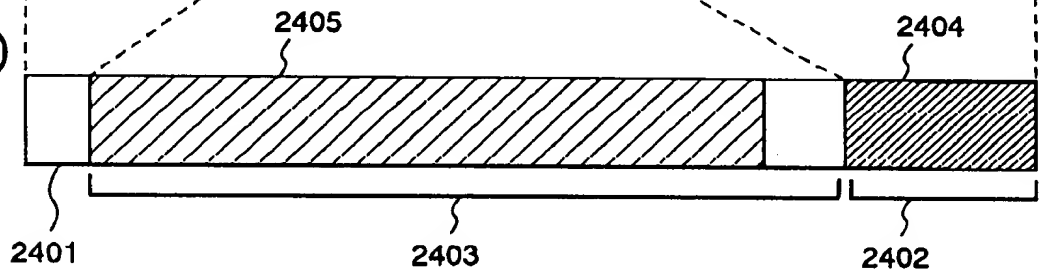
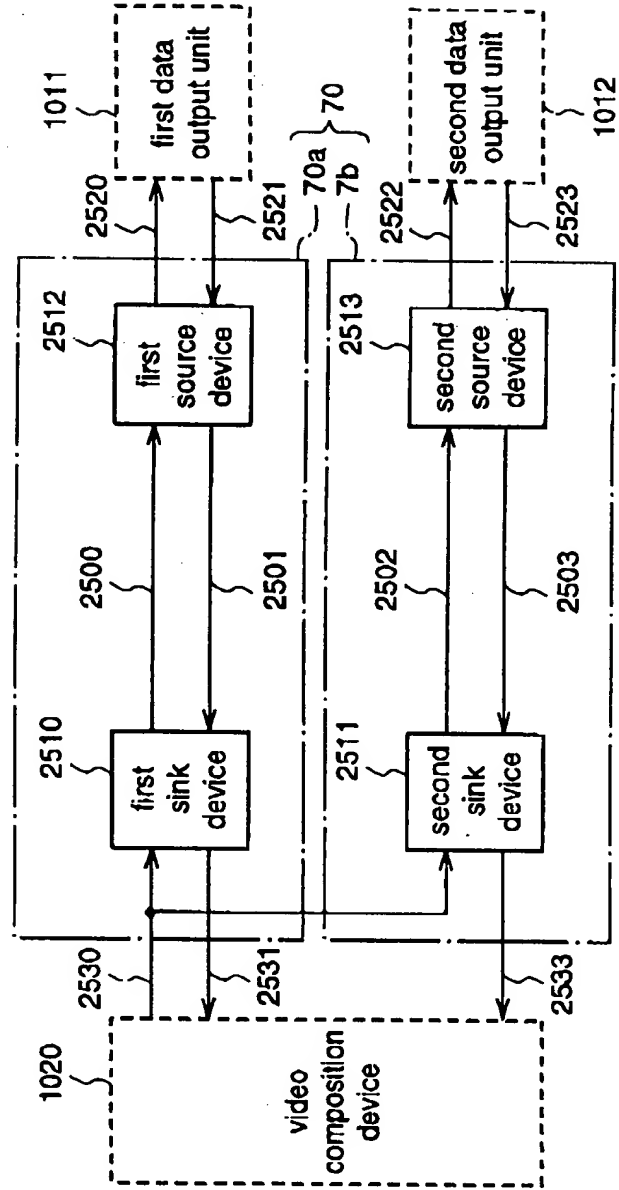


Fig.25



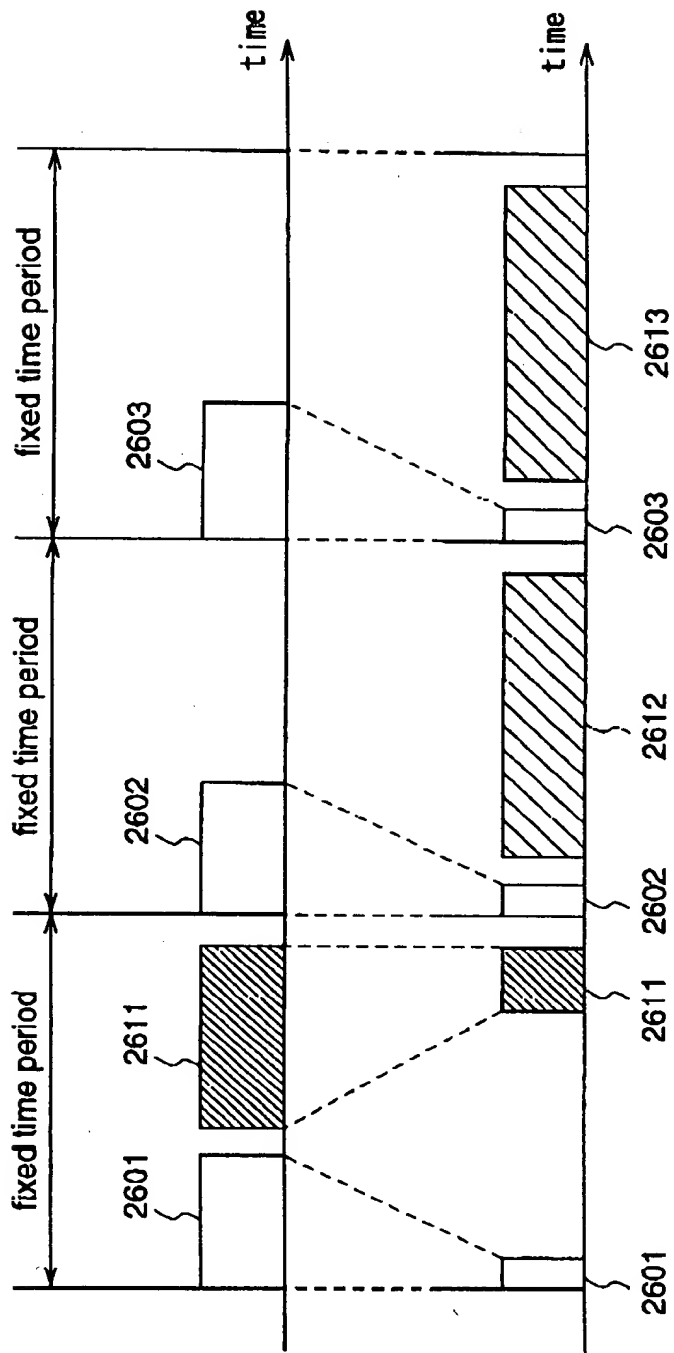


Fig.26 (a)

Fig.26 (b)

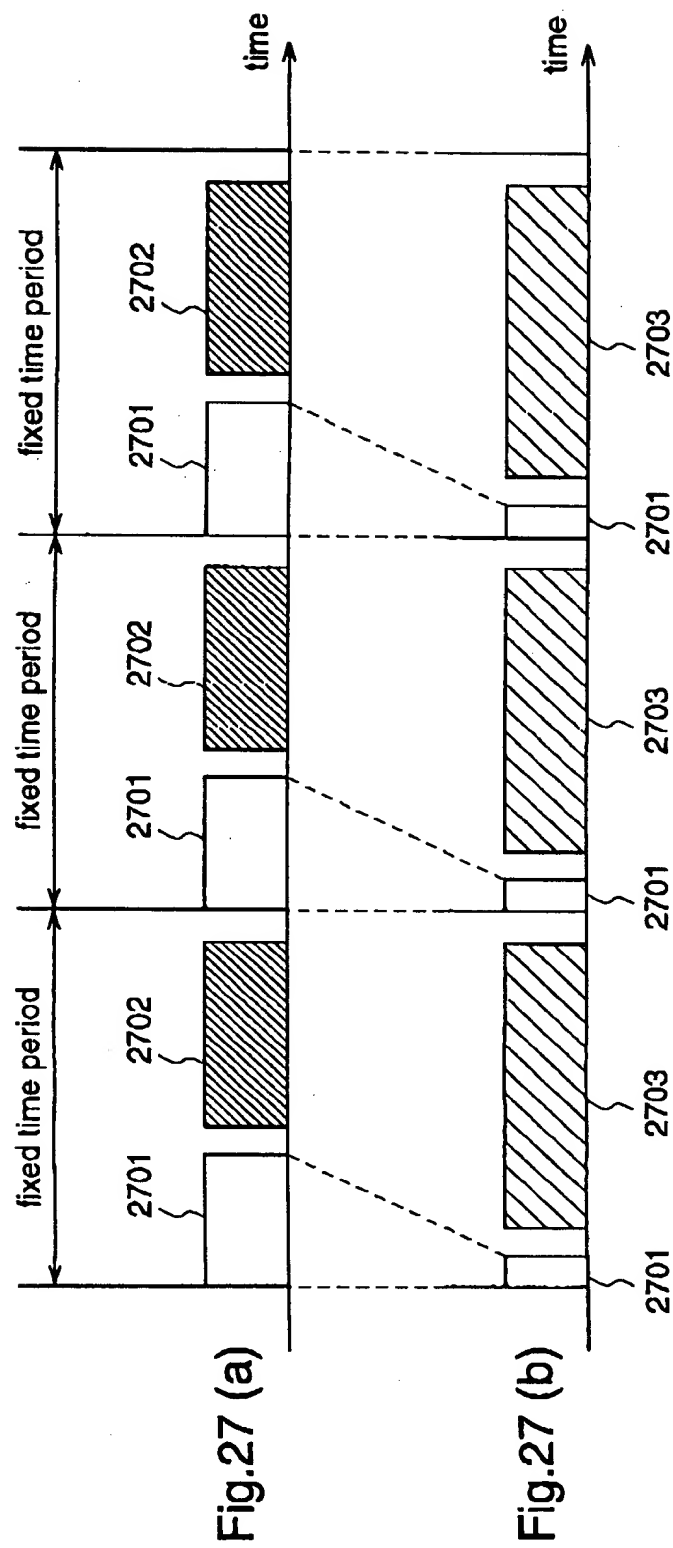


FIG. 28 is a schematic diagram of a semiconductor device in a cross-sectional view, showing a substrate 2801, a gate stack 2802, a gate electrode 2803, a gate insulating layer 2804, and a gate conductive layer 2805.

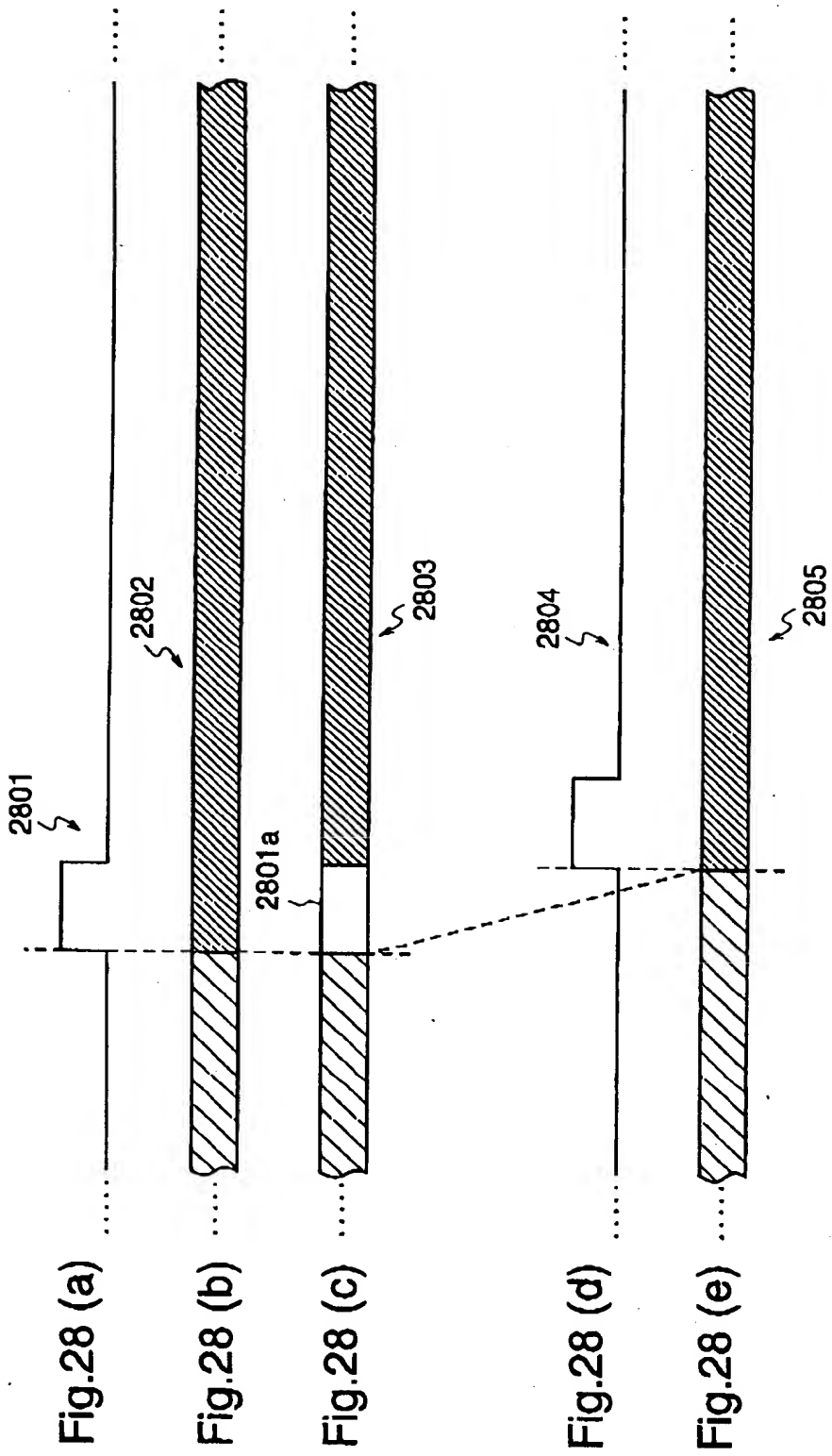


Fig.29 (a)

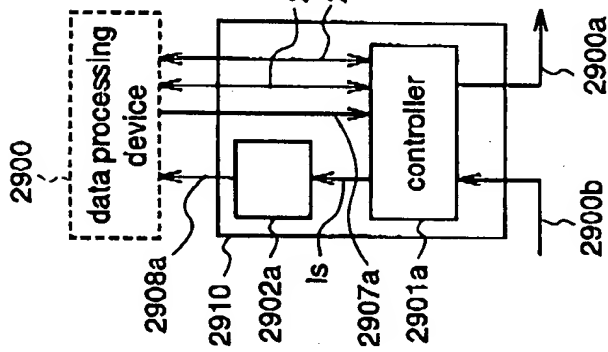


Fig.29 (b)

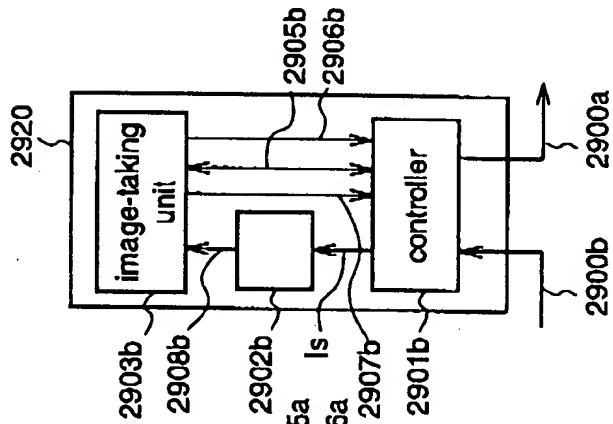


Fig.29 (c)

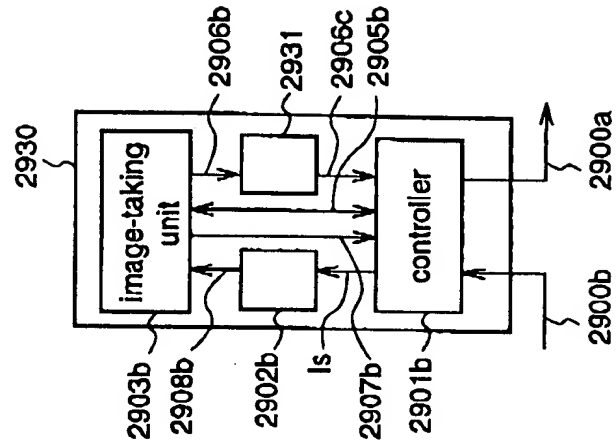


Fig.30 Prior Art

